

**LOYOLA COLLEGE (AUTONOMOUS), CHENNAI – 600 034****B.Sc. DEGREE EXAMINATION – PHYSICS****FIFTH SEMESTER – APRIL 2023****PH 5407 – ELECTRONICS - II**

Date: 12-05-2023

Dept. No.

Max. : 100 Marks

Time: 01:00 PM - 04:00 PM

PART – A**(10x 2 = 20 Marks)**

Q. No.	Answer ALL questions
1	Draw the circuit diagram of logarithmic amplifier.
2	Convert the given hexadecimal number $8E_H$ to a decimal number.
3	State Millman's theorem.
4	What is meant by resolution and accuracy in a D/A converter?
5	Give the difference between JZ and JNZ instructions.
6	Why is the data bus bi-directional?
7	What is phase locked loop?
8	List out the uses of 555 timer.
9	Write an ASM program to multiply two 8-bit numbers in immediate mode of addressing.
10	What are general purpose registers?

PART – B**(4 x 7.5 = 30 Marks)****Answer any FOUR questions**

11	With a neat diagram, explain the working of an Op-Amp as a differentiator.
12	Describe the working of a 3 bit flash A/D convertor.
13	Explain the data transfer and arithmetic instructions of μP 8085.
14	Write an ASM program to divide two 8 bit numbers in indirect mode of addressing.
15	With a neat diagram explain the working of an astable multivibrator using IC 555 timer.
16	Explain with a neat diagram the working of a counter type A/D converter.

PART – C**(4 x 12.5 = 50 Marks)****Answer any FOUR questions**

17	With a circuit diagram explain the working of a 4-bit R-2R ladder D/A converter with Op-Amp.
18	Draw the circuit diagram and explain the working of a second order high pass filter.
19	Explain with a neat diagram the working of a 4 bit binary weighted resistor D/A converter.
20	(a) Write an assembly language program to find the square root of the given number in indirect mode of addressing. (6) (b) Write an assembly language program to find the smallest among 10 numbers in an array. (6.5)
21	Draw the pin configuration of IC 555 timer. With a neat diagram, explain the internal architecture of IC 555 timer with its working.
22	Explain the internal architecture of μP 8085 with a neat diagram.

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